WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

programmable logic circuitry;

embedded processor circuitry comprising a processor; and

shared I/O circuitry coupled to the embedded processor circuitry and the programmable logic circuitry that comprises a plurality of I/O pins which are accessible by the processor and the programmable logic circuitry.

2. The integrated circuit of claim 1 wherein the shared I/O circuitry further comprises a plurality of output driver circuits, each coupled to one of the I/O pins, that drive signals sent to the I/O pins.

3. The integrated circuit of claim 1 wherein the shared I/O circuitry further comprises a plurality of input driver circuits, each coupled to one of the I/O pins, that drive signals received on the I/O pins.

4. The integrated circuit of claim 1 wherein the shared I/O circuitry further comprises:

a first multiplexer coupled to receive a first data signal from the programmable logic circuitry at a first input and a second data signal from the embedded processor circuitry at a second input; and

a driver circuit that drives the output of the first multiplexer onto a first one of the I/O pins.

5. The integrated circuit of claim 4 wherein the first multiplexer selects the first data signal or the second data signal in response to a control signal stored in a register, and wherein the processor can write to the register to gain access to the first I/O pin.

6. The integrated circuit of claim 4 wherein the shared I/O circuitry further comprises JTAG circuitry coupled between the first multiplexer and the driver circuit.

7. The integrated circuit of claim 4 wherein the shared I/O circuitry further comprises:

a second multiplexer coupled to receive an output enable signal from the programmable logic circuitry at a first input and an output enable signal from the embedded

processor circuitry at a second input, wherein the output of the second multiplexer drives a tri-state input of the driver circuit.

8. The integrated circuit of claim 7 wherein JTAG is circuitry coupled between the second multiplexer and the tri-state input of the driver circuit.

9. The integrated circuit of claim 1 wherein the shared I/O circuitry further comprises a plurality of switches that couple signals received at the I/O pins to data input signal lines to the embedded processor circuitry.

10. The integrated circuit of claim 9 wherein the shared I/O circuitry further comprises a plurality of driver circuits coupled to the I/O pins that drive signals received on the I/O pins to the programmable logic circuitry and the embedded processor circuitry.

11. The integrated circuit of claim 10 wherein the shared I/O circuitry further comprises JTAG circuitry coupled between the driver circuits and the switches.

12. The integrated circuit of claim 1 wherein the programmable logic circuitry comprises snoop circuitry that monitors input signals received at the I/O pins and transmitted to the embedded processor circuitry.

13. The integrated circuit of claim 12 wherein the snoop circuitry performs debugging functions on the input signals received at the I/O pins and transmitted to the embedded processor circuitry.

14. The integrated circuit of claim 1 wherein the shared I/O circuitry further comprises a plurality of multiplexers which select from a first plurality of control signals from the programmable logic circuitry and a second plurality of control signals from the embedded processor circuitry to provide a third plurality of control signals which determine an I/O standard for the shared I/O circuitry.

15. The integrated circuit of claim 1 wherein data bits are loaded into the programmable logic circuitry through the I/O pins of the shared I/O circuitry to configure the programmable logic circuitry.

16. The integrated circuit of claim 1 wherein the integrated circuit further comprises a power up mode during which the I/O pins in the shared I/O circuitry are accessible by the programmable logic circuitry by default.

17. The integrated circuit of claim 1 wherein the shared I/O circuitry loads data bits into the programmable logic circuitry and the processor during a Boot from Flash Mode.

18. The integrated circuit of claim 1 wherein the shared I/O circuitry alternately loads a stream of data bits received at the I/O pins into the processor and the programmable logic circuitry.

19. An integrated circuit, comprising:

a programmable logic portion comprising a plurality of I/O pins;

a processor; and

shared I/O circuitry that provides circuitry in the programmable logic portion and the processor with signal access to the I/O pins.

20. A method for transmitting data signals to and from an integrated circuit, the method comprising:

transmitting a first input signal received at an I/O pin to programmable logic circuitry on the integrated circuit;

transmitting a second input signal received at the I/O pin to a processor on the integrated circuit;

transmitting a first output signal from the programmable logic circuitry to the I/O pin; and

transmitting a second output signal from the processor to the I/O pin.

21. The method of claim 20 wherein transmitting the second input signal received at the I/O pin to the processor further comprises maintaining a switch ON.

22. The method of claim 20 wherein transmitting the first output signal from the programmable logic circuitry to the I/O pin further comprises selecting the first output signal using a first multiplexer and applying an output signal of the first multiplexer to a driver circuit.

23. The method of claim 22 wherein transmitting the first output signal from the programmable logic circuitry to the I/O pin further comprises selecting an output enable signal from the programmable logic circuitry using a second multiplexer and applying an output signal of the second multiplexer to a tri-state input of the driver circuit.

24. The method of claim 20 wherein transmitting the second output signal from the processor to the I/O pin further comprises selecting the second output signal using a first multiplexer and applying an output signal of the first multiplexer to a driver circuit.

25. The method of claim 24 wherein transmitting the second output signal from the processor to the I/O pin further comprises selecting an output enable signal from the processor using a second multiplexer and applying an output signal of the second multiplexer to a tri-state input of the driver circuit.

26. The method of claim 20 further comprising selecting a first control signal from the programmable logic circuitry or a second control signal from the processor to set an I/O standard for the I/O pin.

27. The method of claim 20 wherein transmitting the first input signal received at the I/O pin to the programmable logic circuitry further comprises monitoring signals received at the I/O pin and transmitted to the processor.

28. A method for augmenting the functionality of an integrated circuit comprising programmable logic circuitry, the method comprising:

adding a processor to the integrated circuit;

adding shared I/O pins to the integrated circuit; and

adding a first plurality of multiplexing circuits to the integrated circuit that control access to the I/O pins by data signals from the programmable logic circuitry and the processor.

29. The method of claim 28 further comprising:

adding a second plurality of multiplexing circuits that select signals from the processor and the programmable logic circuitry which determine an I/O standard for the shared I/O pins.

30. The method of claim 28 further comprising:

adding output drivers to each of the shared I/O pins which drive the data signals from the programmable logic circuitry and the processor to the shared I/O pins; and

adding input drivers to each of the shared I/O pins which drive signals received at the I/O pins to the programmable logic circuitry and the processor to the shared I/O pins.

31. The method of claim 28 further comprising:

selecting a first data signal from the programmable logic circuitry or a second data signal from the processor to be transmitted to a first one of the shared I/O pins using one of the multiplexing circuits which is controlled by a control signal stored in a register, wherein the processor can write to the register to gain access to the first shared I/O pin.

32. The method of claim 28 wherein the first plurality of multiplexing circuits select enable signals from the programmable logic circuitry or the processor, the enable signals determining whether the programmable logic circuitry or the processor accesses the shared I/O pins.

33. An integrated circuit, comprising:

a programmable logic portion;

an embedded logic portion adjacent to a first edge of the integrated circuit, the embedded logic portion comprising a processor; and

a shared I/O portion in between the programmable logic portion and the embedded logic portion, the shared I/O portion comprising first I/O pins that are accessible by circuitry in the programmable logic portion and the embedded logic portion.

34. The integrated circuit of claim 33 further comprising a fourth portion that includes second I/O pins adjacent to second, third, and fourth edges of the integrated circuit.

35. The integrated circuit of claim 34 wherein the programmable logic portion is surrounded by the shared I/O and the fourth portions of the integrated circuit.

36. The integrated circuit of claim 33 further comprising a fourth portion of the integrated circuit adjacent to the shared I/O portion that comprises first multiplexers which select data signals from the programmable logic portion and the embedded logic portion to be driven onto the first I/O pins.

37. The integrated circuit of claim 36 wherein the fourth portion of the integrated circuit further comprises second multiplexers which select I/O standard signals from the programmable logic portion and the embedded logic portion.

38. A method for operating an integrated circuit comprising a programmable logic portion, a processor portion having a processor, and I/O pins that are accessible by the programmable logic portion and the processor portion, the method comprising:

transmitting input signals received at the I/O pins to the programmable logic portion during power up of the integrated circuit; and

transmitting output signals from the programmable logic portion to the I/O pins during the power up of the integrated circuit.

39. A method for operating an integrated circuit comprising a programmable logic portion, a processor portion having a processor, and I/O pins that are accessible by the programmable logic portion and the processor portion, the method comprising:

accessing bits stored in a Flash interface external to the integrated circuit to obtain boot code for the processor using the I/O pins; and

accessing bits stored in the Flash interface for the programmable logic portion using the I/O pins.

40. A method for operating an integrated circuit comprising a programmable logic portion, a processor portion having a processor, and I/O pins that are accessible by the programmable logic portion and the processor portion, the method comprising:

transmitting data bits through some of the I/O pins to configure circuitry within the programmable logic portion; and

transmitting data bits through some of the I/O pins to configure circuitry within the processor.

41. A method for operating an integrated circuit comprising a programmable logic portion, a processor portion having a processor, and I/O pins that are accessible by the programmable logic portion and the processor portion, the method comprising:

transmitting a first signal stream received at a first of the I/O pins to circuitry in the programmable logic portion; and

transmitting a second signal stream received at the first I/O pin to circuitry in the processor portion concurrently with the first signal stream.

42. The method of claim 41 wherein transmitting the second signal stream further comprises switching a switch ON and OFF in response to a control signal to dynamically toggle signals received at the first I/O pin between the circuitry in the programmable logic portion and the circuitry in the processor portion.